Book Review 1

High Performance VLSI Signal Processing: Innovative Architectures and Algorithms

Volume I - Algorithms and Architectures
Edited by K. J. Ray LIU and Kung YAO. IEEE Press. 1998
ISBN 0-7803-3468-X

Modern signal processing technology involves interaction among areas such as VLSI and circuit design, computer architecture, signal processing, communications and computer-aided design.

The book intends to address the important aspects of high-performance signal processing with a focus on the recent development of VLSI technology for signal processing.

The editors collect much of all the research efforts and findings that have made high performance implementation of signal processing possible in the last decade in two volumes.

In Volume I, the editors cover issues related to system design and methodology. They have selected 40 papers -from journal publications only- grouped in five chapters. Each chapter has a precise and well-referenced introduction, describing the evolution of the topic, followed by selected papers reprints.

Chapter I - Array Processors and Mapping, deals with the fundamental concepts and designs of systolic/wavefront, concurrent, and parallel VLSI array processors which serve as the platforms for high-performance signal processing. Reprinted papers begin with motivational and tutorial H. T. Kung´s paper, *Why Systolic Architectures?* (IEEE Computer, January 1982) and among others we have *On the Design of Algorithms for VLSI Systolic Arrays,* D. Moldovan (Proceedings of the IEEE, January 1983), *Regular Iterative Algorithms and their Implementation on Processor Arrays,* S. Rao and T. Kailath (Proceedings of the IEEE, March 1988) and *Optimization of Computation Time for Systolic Arrays,* Y. Wong and J. Delosme (IEEE Transactions on Computers, February 1992).

Chapter 2 - Transformation and Design Techniques, it considers methodologies concerning systematic transformation and mapping, from algorithm to architectures, and techniques used to improve concurrent pipelined processing. This chapter starts with an excellent tutorial paper by K. K. Parhi *Algorithm Transformation Techniques for Concurrent Processors* (Proceedings of the IEEE, December 1989), other papers are on optimum unfolding, look-ahead computations or data flow processing.

In Chapter 3 - Computer-Aided Designs, which develops automatic design tools for signal processing, deals with Silicon compilers and their necessary tools are introduced. First, a tutorial by McFarland, Parker and Camposano explores *The High-Level Synthesis of Digital Systems* (Proceedings of the IEEE, February 1990), then papers on specialized DSP silicon compilers and synthesis for VLSI

implementation follow. Design and simulation of heterogeneous systems, and scheduling to efficient implementation of DSP algorithms on multiprocessors systems are the last items treated.

Chapter 4 - System Architecture and Implementation, presents implementational schemes and computing systems designs suited for signal processing architectures. Main examples of reprinted papers are *The Warp Computer Architecture, implementation, and Performance* by M. Annaratone et al. (IEEE Transactions on Computers, December 1987) and *CORDIC-based VLSI Architectures for Digital Signal Processing* by Y. H. Hu (IEEE Signal Processing, July 1992).

Chapter 5 - Fault Tolerance in VLSI Signal Processing, considers fault-tolerance techniques for improvement reliability of VLSI signal processing systems. Fault (error) detection, fault diagnosis and fault recovery are the three main functions of a fault tolerance system, the former being the most important in real time signal processing. Algorithm-based fault-tolerance is the focus of the reprinted papers including an excellent tutorial paper by Chean and Fortes *A Taxonomy of Reconfiguration Techniques for Fault-Tolerant Processor Arrays* (IEEE Computer, January 1990)

This book is especially appropiate for someone who has a basic understanding of signal processing and is interested in high-performance implementation of signal/image processing, including those with analytical, system, software, or hardware interests in this area.

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